REMARKS

File History

The present application is a continuation of, and claims benefit pursuant to 35 USC §120 of, U.S. Patent Application No. 10/071,689 filed February 8, 2002 (hereafter also, "parent application").

During prosecution of the parent application, a restriction requirement was made, the method claims were elected, and various anticipation or obviousness rejections were made on the basis of one or more of the following references:

Previously Applied References

Takeuchi (U.S. 5,661,056)

Hagiwara (U.S. 5,847,427)

Lin (U.S. 6,127,227)

Misium (U.S. 6,261,973)

George Misium ("George", U.S. 6,140,024)

Furukawa (U.S. patent application 2002/0185675)

Chou (U.S. 6,426,305)

Newly cited documents (not previously cited)

Crivelli (U.S. Application 2003-0183869 published October 2, 2003, filed January 30, 2003 as Serial No.: 356,351 Series Code: 10)

Chen (U.S. Application 2003-0232507 published Dec. 18, 2003, filed June 12, 2002 as Serial No.: 167,821 Series Code: 10)

The previous rejections can be loosely summarized as maintaining that various forms of nitridations, including ion implantation of nitrogen, thermal nitridation in a nitrogen containing atmosphere, RPN, DPN, and so forth, are fully interchangeable and the ordinary artisan would have been motivated to swap any one for the other in all circumstances and/or at all times.

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The previous rejections can further be loosely summarized as maintaining that various ways of forming silicon oxide, including thermal oxidation, ion implantation of oxygen, CVD deposition, and so forth are fully interchangeable and the ordinary artisan would have been motivated to swap any one for the other in all circumstances and/or at all times.

Applicants respectfully submit that these underpinnings of rejections are incorrect and deserve to be reviewed and re-evaluated.

The viewpoint of the ordinary artisan has changed over time. What may have been conventional practice in pre-submicron days is no longer seen as conventional. The motivational directions of artisans has changed over time. In the early days of semiconductor production, thermal budget was not as big a concern as it has become more recently. The rising concern for thermal budgets has colored the way modern artisans view the practice, this coloration being present at the time of invention of the present subject matter AND EVEN LATER (-- Applicants will shortly show "evidence" that the last part is true).

Consider first, the **Misium reference (U.S. 6,261,973)** which was applied in the parent application. Misium '973 is based on a provisional filed in late 1997 and shows that even by that date, practitioners were concerned with thermal budget. Misium '973 states at col. 1, lines 54-62: "The thermal budget must be lowered to e.g., enable scaling of high density integrated circuits. In addition, the large number of high temperature processing steps cause a significant impact on energy consumption and environmental impact of ... " (emphasis added).

Misium '973 must be read in whole for what it fairly teaches: namely that 1) thermal budget must be lowered and 2) energy consumption should be lowered. Moreover, it must be recognized that Misium '973 is using RPN (col. 4, line 26) for the primary purpose of creating a surface-based "etch stop" (col. 4, line 27) that protects, among other things, the oxide sidewalls (32) of the structure of Fig. 3C from the HF wet etch (see col. 3, line 50). Misium '973 nowhere teaches or suggests that RPN should be used for improving dielectric properties of an inter-gates insulator in a floating gate memory device. Accordingly, Misium '973 is silent as to use of RPN for improving dielectric properties AND Misium '973 teaches away from processes that do not minimize thermal budget AND Misium '973 teaches away from processes that increase energy consumption. (Admittedly, at col. 5, line 21, and with limited application to the "trench isolation" of Fig. 5F, Misium '973 does indicate that high

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temperature oxidizing may follow, but only where "required". Those skilled in the art will appreciate that the "trench isolation" step of Fig. 5F comes very early in processing, typically before gate oxide is thermally grown. Thus Misium '973 cannot be fairly read by skilled artisans as suggesting that thermal oxidation should be carried out later and again in processing, particularly in view of Misium's admonitions against increasing of thermal budget and of energy consumption.)

Next consider **Lin (U.S. 6,127,227)** which was also applied in the parent application. Lin '227 was filed in early 1999 and demonstrates what the ordinary artisan's thinking was in the area of ONO stack formation for flash memory (see title of invention). Lin '227 teaches that ion implantation should be used (Fig. 2B) so as to provide an oxidation "stop" layer at a certain depth (125) below the surface of the polysilicon layer (120). More specifically, it is Lin's directions and expectations that the polysilicon material (~143) above the high-energy implanted nitrogen atoms (125) should be easily and rapidly oxidized to form a "bottom oxide [having] a thickness of between about 40 and 120Å" (col. 4, lines 66-67) while the implanted nitrogen atoms layer (125) is "simultaneously" converted to an "augmented" thin layer (130) which is composed of a combination of Si, N and O atoms (col. 4, lines 62-66) having a thickness of "only between about 5 to 10Å". Lin '227 does not anywhere suggest or show appreciation for the idea that the structure he calls the "augmented" thin layer (130) should be created by itself without the "simultaneously" formed bottom-oxide (143) which lies above layer 130 and has a thickness of between about 40 and 120Å.

RPN or DPN are not interchangeable with the ion implantation process taught by Lin '227. First, ion implantation is a higher energy process because it seeks to implant the nitrogen atoms (in this case) deep below the exposed surface of the wafer (e.g., to level 125 of Lin's Fig. 2B for example). It is a "punch-through" technology. By contrast, RPN or DPN are relatively low energy process because they seek to incorporate nitrogen atoms primarily into the exposed surface of the wafer, not deep below it.

Second, the concentration of nitrogen atoms that may be practically implanted deep below the exposed surface of the wafer via ion implantation tends to be substantially less than the concentration of nitrogen atoms that may be practically incorporated at the exposed surface of the wafer via RPN or DPN because the latter processes (RPN or DPN) are surface

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processes that do not have to force the nitrogen atoms substantially below the surface silicon atoms as does ion implantation.

Third, and this is an extension of the second aspect, surface processes such as RPN or DPN do not create crystal defects in the targeted silicon layer because they do not seek to force the nitrogen atoms substantially below the surface silicon atoms as does the ion implantation process. By contrast, ion implantation inherently introduces defects into the overlying silicon material specifically because it does seek to force the nitrogen atoms substantially below the surface silicon atoms.

It is demonstrated by the above that RPN or DPN are not the same as ion implantation of nitrogen atoms. An ordinary artisan would not see them at the relevant time as being interchangeable.

Now let us leap frog in time to the year 2003. This is when the here submitted, new piece of evidence was filed as a patent application: **Crivelli United States Patent Application 2003-0183869** published October 2, 2003, filed January 30, 2003 as Serial No.: 356351 Series Code: 10 ("Manufacturing process of an interpoly dielectric structure for non-volatile semiconductor integrated memories"). Of importance note that Crivelli '2003 was filed almost a year after the filing date of the parent application from which benefit is here claimed.

Figure 5 of Crivelli shows a surface-nitrided layer (5) of a Floating Gate (FG, 4) where RPN is one of the methods taught for nitriding the FG surface. An ONO stack is provided on top of the surface-nitrided layer (5).

Despite its apparent closeness, Crivelli fails to teach or suggest the idea of thermally oxidizing the surface-nitrided layer (5). Instead they form the ONO stack with conventional CVD above the surface-nitrided layer (5).

Crivelli is a person of ABOVE-ordinary skill in the art because she has been issued at least one patent in the EEPROM arts: 6,319,780. Despite this high level of skill, the later-filing Crivelli et al. failed to see the advantages of the here claimed method. Crivelli et al. pile a conventional ONO stack by CVD on top of the surface-nitrided layer (5) without thermally oxidizing the layer 5. The question is why and the answer is because of thermal budget. The

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modern thinking is to avoid high temperature processing wherever possible. (Picking and choosing is the road sign of hindsight; e.g., "Let's raise it here but lower it there.")

RPN and DPN are nitrogen introduction techniques of relatively low energy and low temperature and they are directed to providing nitridation of only a surface, not deep under it. An artisan who is employing RPN or DPN is thinking of it as a surface coating process. An artisan who is employing RPN or DPN is thinking of its advantageous properties of relatively low energy and low temperature. It would go against modern thinking to employ a high energy, high temperature process such as thermal oxidation at a processing stage after the gate oxide and floating gate have been created.

Request for Examination

Examination is respectfully requested for the amended application. A telephone call to the below attorney is requested if it will help expedite processing of the application.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time and/or fee for additional claims, which may be required.

Respectfully submitted,

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APPENDIX (Jan. 2004)

CLEAN COPY OF AMENDED, NON-AMENDED AND NEW CLAIMS

1. (*Currently amended*) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

(a) forming a conductive first layer containing primarily silicon, the first layer being to provide one or more floating gates for the nonvolatile memory;

(b) nitriding a silicon-containing surface of the first layer with a low temperature, low energy, surface nitriding process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said silicon-containing surface of the first layer at relatively low temperature and relatively low energy;

(c) subjecting the nitrided surface to a thermally oxidizing atmosphere so as to thereby form a thermally-grown silicon oxide at the nitrided surface, the combination of the thermally-grown silicon oxide and incorporated nitrogen atoms defining at least part of a first dielectric of the nonvolatile memory; and

(d) forming a conductive second layer separated by the first dielectric from conductive material of the first layer, the conductive second layer providing one or more control gates for the nonvolatile memory.

2. (*Currently amended*) The method of Claim 1 wherein forming the silicon oxide at the nitrided surface comprises performing oxidation at a temperature in the range 800°C-1050°C in an oxygen or oxygen/hydrogen atmosphere to thereby form the silicon oxide by thermal oxidation.

3. (*Original*) The method of Claim 1 wherein the surface of the first layer is a polysilicon surface.

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4. (*Canceled*)

5. (*Canceled*)

6. (*Canceled*)

7. (*Canceled*)

8. (*Canceled*)

9. (*Canceled*)

10. (New) The method of Claim 1 wherein the nitriding step includes using a Remote Plasma Nitridation (RPN) process.

11. (New) The method of Claim 1 wherein the nitriding step includes using a Decoupled Plasma Nitridation (DPN) process.

12. (New) The method of Claim 1 wherein the nitriding step provides a concentration of nitrogen atoms of 1-20 atomic percent in the nitrided surface.

13. (New) The method of Claim 12 wherein the nitriding step incorporates said nitrogen atoms to a depth of no more than 3 nm in said surface of the first layer.

14. (New) The method of Claim 1 wherein said first layer is disposed over a tunneling dielectric.

15. (New) The method of Claim 14 and further comprising: thermally growing the tunneling dielectric.

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16. (New) The method of Claim 1 and further comprising: depositing a silicon nitride layer on said combination of the thermally-grown silicon oxide and incorporated nitrogen atoms to thereby define a further part of the first dielectric of the nonvolatile memory.

17. (New) The method of Claim 16 and further comprising: depositing a silicon oxide layer on said deposited silicon nitride layer to thereby define a yet further part of the first dielectric of the nonvolatile memory.

18. (New) A method of manufacturing a nonvolatile memory cell within a monolithically integrated circuit, the method comprising:

(a) forming a tunneling dielectric layer on a semiconductive substrate;

(b) forming a floating gate layer on said tunneling dielectric layer, the floating gate layer having a top surface composed primarily of conductive silicon;

(c) surface nitridating said top surface of the floating gate layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said top surface of the floating gate layer at relatively low temperature and relatively low energy; and

(d) subjecting the nitrided top surface to a thermally oxidizing atmosphere so as to thereby form a combination of thermally-grown silicon oxide and surface incorporated and thermally treated nitrogen atoms at the nitrided and thermally oxidized top surface of the floating gate layer.

19. (New) The memory cell manufacturing method of Claim 18 and further comprising:

(e) depositing a silicon nitride layer directly on the nitrided and thermally oxidized top surface of the floating gate layer.

20. (New) The memory cell manufacturing method of Claim 19 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

21. (New) The memory cell manufacturing method of Claim 19 and further comprising:

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(f) depositing a silicon oxide layer directly on the silicon nitride layer.

22. (New) The memory cell manufacturing method of Claim 21 and further comprising:

(g) surface nitridating said deposited silicon oxide layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said deposited silicon oxide layer at relatively low temperature and relatively low energy.

23. (New) The memory cell manufacturing method of Claim 22 and further comprising:

(h) forming a conductive gate layer on said surface nitridated and deposited silicon oxide layer.

24. (New) The memory cell manufacturing method of Claim 18 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

25. (New) The memory cell manufacturing method of Claim 18 and further wherein:

said surface nitridating step incorporates nitrogen atoms into the said top surface of the floating gate layer to a depth of less than 3nm.

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CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a continuation of, and claims benefit of, U.S. Patent Application No. 10/071,689 filed February 8, 2002, whose entire disclosure is incorporated herein by reference.

Page 3, lines 11-18, is as follows:

Fig. 2 illustrates a cross section of a nonvolatile memory cell at an early stage of fabrication. Semiconductor substrate 120 (monocrystalline silicon or some other material) is processed to form a suitably doped channel region 150 (type P in Fig. 2, but an N type channel can also be used). Dielectric 130 is formed on substrate 120 over channel 150. Dielectric 130 may be thermally grown silicon dioxide or some other type of dielectric. Then polysilicon layer 110 is deposited and doped during or after deposition. See for example U.S. patent application 09/640,139 filed August 15, 2000 and incorporated herein by reference (now U.S. patent no. 6,355,524 issued March 12, 2002).

Page 5, lines 12-22, is as follows:

Known techniques can be used to complete the memory fabrication. In the example of Fig. 4, silicon nitride layer 410 is formed by low pressure CVD (LPCVD) on layer 310. Silicon dioxide 420 is deposited by CVD, or thermally grown, on layer 410. Layers 310, 410, 420 are referenced as 160. Doped polysilicon 170, or some other conductive material, is deposited to provide the control gates (possibly wordlines each of which provides the control gates for a row of memory cells). The layers 170, 420, 410, 310, 110, 130 are patterned as needed. Source/drain regions 140 are formed by doping. Additional layers (not shown) may be formed to provide select gates, erase gates, or other features. See the aforementioned U.S. patent no. 6,355,524 for an exemplary memory fabrication process that can be modified to incorporate the floating gate nitridation described above.

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